

Dual 4-Stage Binary Ripple Counter

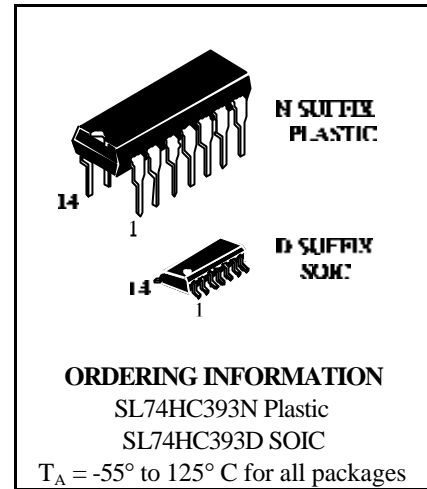
High-Performance Silicon-Gate CMOS

The SL74HC393 is identical in pinout to the LS/ALS393. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

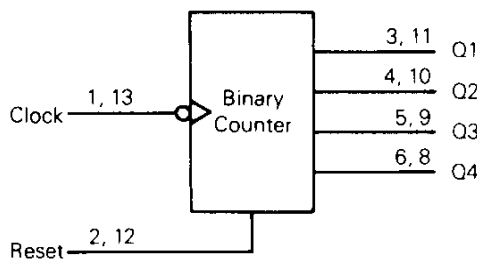
This device consists of two independent 4-bit binary ripple counters with parallel outputs from each counter stage. A ÷256 counter can be obtained by cascading the two binary counters.

Internal flip-flops are triggered by high-to-low transitions of the clock input. Reset for the counters is asynchronous and active-high. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used as clocks or as strobes except when gated with the Clock of the SL74HC393.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices



LOGIC DIAGRAM



PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

Clock a	1	14	V_{CC}
Reset a	2	13	Clock b
$Q1_a$	3	12	Reset b
$Q2_a$	4	11	$Q1_b$
$Q3_a$	5	10	$Q2_b$
$Q4_a$	6	9	$Q3_b$
GND	7	8	$Q4_b$

FUNCTION TABLE

Inputs		Outputs
Clock	Reset	
X	H	L
H	L	No Change
L	L	No Change
	L	No Change
	L	Advance to Next State

X = don't care

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin	±20	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)			
	V _{CC} =2.0 V	0	1000	ns
	V _{CC} =4.5 V	0	500	
	V _{CC} =6.0 V	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.



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DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.3	0.3	0.3	V
			4.5	0.9	0.9	0.9	
			6.0	1.2	1.2	1.2	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
		6.0	5.9	5.9	5.9		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
6.0	5.48		5.34	5.2			
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
		6.0	0.1	0.1	0.1		
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
6.0	0.26		0.33	0.4			
I _{IN}	Maximum Input Leakage Current	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current (per Package)	V _{IN} =V _{CC} or GND I _{OUT} =0μA	6.0	8.0	80	160	μA



AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 3)	2.0	5.4	4.4	3.6	MHz
		4.5	27	22	18	
		6.0	32	26	21	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q1 (Figures 1 and 3)	2.0	120	150	180	ns
		4.5	24	30	36	
		6.0	20	26	31	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q2 (Figures 1 and 3)	2.0	190	240	285	ns
		4.5	38	48	57	
		6.0	32	41	48	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q3 (Figures 1 and 3)	2.0	240	300	360	ns
		4.5	48	60	72	
		6.0	41	51	61	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q4 (Figures 1 and 3)	2.0	290	365	435	ns
		4.5	58	73	87	
		6.0	49	62	74	
t _{PHL}	Maximum Propagation Delay, Reset to any Q (Figures 2 and 3)	2.0	165	205	250	ns
		4.5	33	41	50	
		6.0	28	35	43	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 3)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C _{IN}	Maximum Input Capacitance	-	10	10	10	pF

C _{PD}	Power Dissipation Capacitance (Per Counter)	Typical @25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	40			

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to-55°C	≤85°C	≤125°C	
t _{rec}	Minimum Recovery Time, Reset Inactive to Clock (Figure 2)	2.0	50	65	75	ns
		4.5	10	13	15	
		6.0	9	11	13	
t _w	Minimum Pulse Width, Clock (Figure 1)	2.0	80	100	120	ns
		4.5	16	20	24	
		6.0	14	17	20	
t _w	Minimum Pulse Width, Set (Figure 2)	2.0	125	155	190	ns
		4.5	25	31	38	
		6.0	21	26	32	
t _r , t _f	Maximum Input Rise and Fall Times (Figure 1)	2.0	1000	1000	1000	ns
		4.5	500	500	500	



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		6.0	400	400	400	
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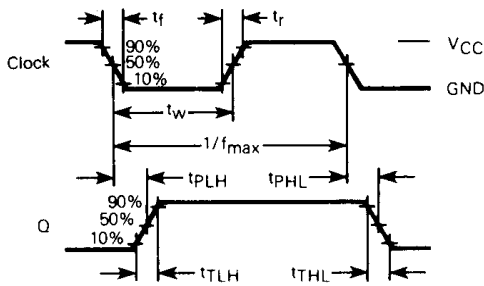


Figure 1. Switching Waveform

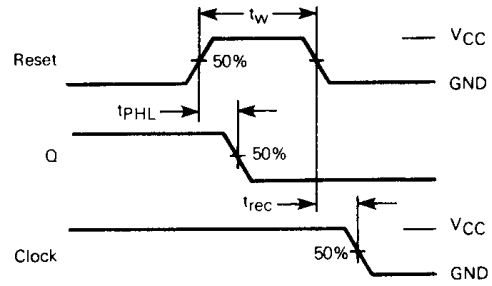
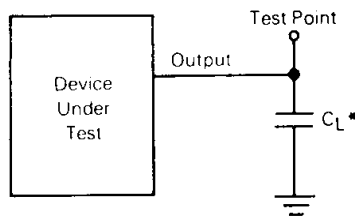


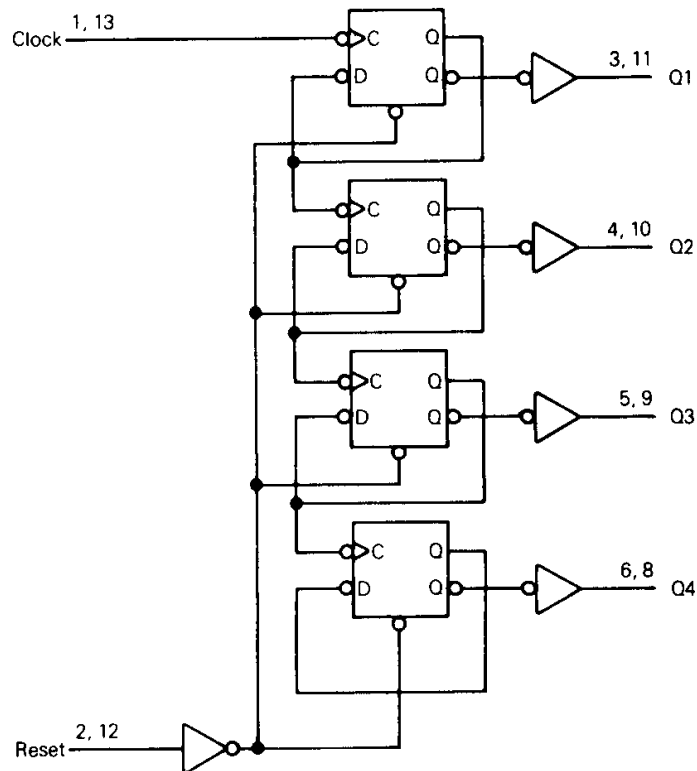
Figure 2. Switching Waveform



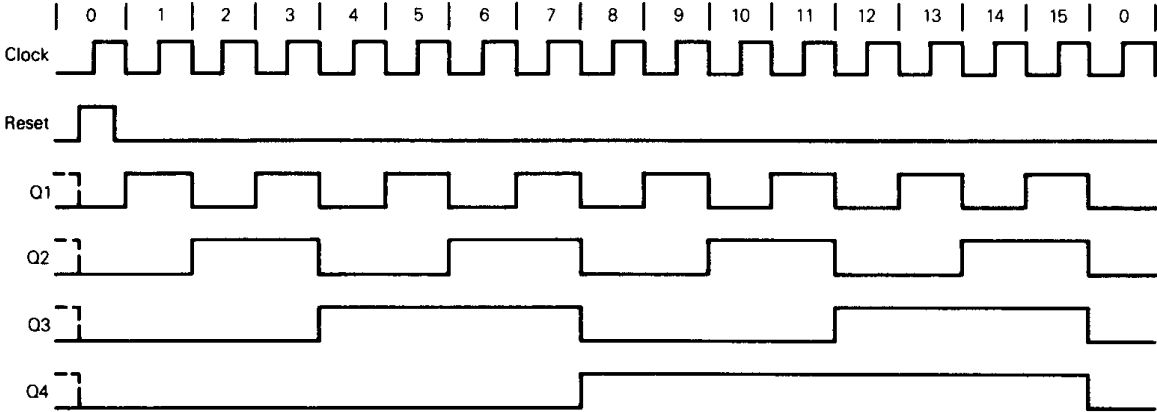
* Includes all probe and jig capacitance

Figure 4. Test Circuit

EXPANDED LOGIC DIAGRAM



TIMING DIAGRAM



COUNT SEQUENCE

Count	Outputs			
	Q4	Q3	Q2	Q1
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H