

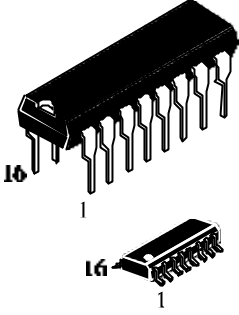
Dual Monostable Multivibrator

The SL74HC221 is identical in pinout to the LS/ALS221. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LS/ALSTTL outputs.

There are two trigger inputs, \overline{A} INPUT (negative edge) and B INPUT (positive edge). These inputs are valid for rising/falling signals

The device may also be triggered by using the CLR input (positive-edge) because of the Schmitt-trigger input; after triggering the output maintains the MONOSTABLE state for the time period determined by the external resistor R_x and capacitor C_x . Taking CLR low breaks this MONOSTABLE STATE. If the next trigger pulse occurs during the MONOSTABLE period it makes the MONOSTABLE period longer.

- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 3.0 to 6.0 V
- Low Input Current: 1.0 μ A
- High Noise Immunity Characteristic of CMOS Devices

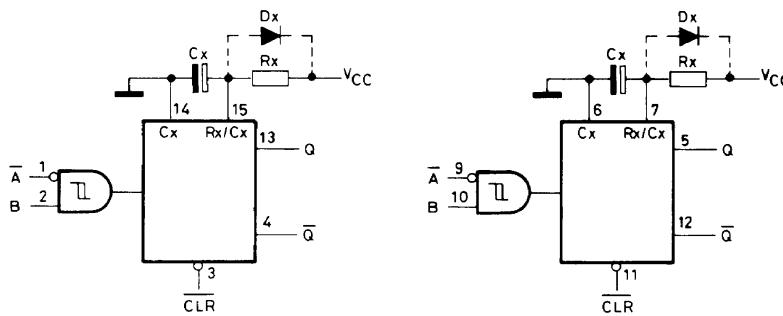


V SUFFIX PLASTIC

D SUFFIX SOIC

ORDERING INFORMATION
 SL74HC221N Plastic
 SL74HC221D SOIC
 $T_A = -55^\circ$ to 125° C for all packages

LOGIC DIAGRAM



PIN 16 = V_{CC}
 PIN 8 = GND

PIN ASSIGNMENT

\overline{A}	1	16	V_{CC}
B	2	15	\overline{BEXT} CLK
\overline{CLR}	3	14	\overline{QEXT}
\overline{Q}	4	13	Q
Q	5	12	\overline{Q}
\overline{AEXT}	6	11	\overline{BEXT}
$\overline{BEXT}/\overline{QEXT}$	7	10	B
GND	8	9	\overline{A}

FUNCTION TABLE

Inputs			Outputs		Note
\overline{A}	B	\overline{CLR}	Q	\overline{Q}	
	H	H			Output Enable
X	L	H	L*	H*	Inhibit
H	X	H	L*	H*	Inhibit
L		H			Output Enable
L	H				Output Enable
X	X	L	L	H	Inhibit

X = don't care
 * - except for monostable period

Note

- (1) C_x , R_x , D_x are external components.
- (2) D_x is a clamping diode.

The external capacitor is charged to V_{CC} in the stand-by state, i.e. no trigger. When the supply voltage is turned off C_x is discharged mainly through an internal parasitic diode. If C_x is sufficiently large and V_{CC} decreases rapidly, there will be some possibility of damaging the I.C. with a surge current or latch-up. If the voltage supply filter capacitor is large enough and V_{CC} decrease slowly, the surge current is automatically limited and damage the I.C. is avoided. The maximum forward current of the parasitic diode is approximately 20 mA.

SL74HC221

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{IN}	DC Input Voltage (Referenced to GND)	-1.5 to V _{CC} +1.5	V
V _{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} +0.5	V
I _{IN}	DC Input Current, per Pin A, B, CLR C _X , R _X	±20 ±30	mA
I _{OUT}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.
 +Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
 SOIC Package: - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	3.0 **	6.0	V
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	-55	+125	°C
t _r , t _f	Input Rise and Fall Time - CLR (Figure 2)	V _{CC} =2.0 V 0 V _{CC} =4.5 V 0 V _{CC} =6.0 V 0	1000 500 400	ns
	A or B	-	No Limit	
R _X	External Timing Resistor	V _{CC} < 4.5 V 10 V _{CC} ≥ 4.5 V 2.0	1000 1000	kΩ
C _X	External Timing Capacitor	0	No Limit	μF

** The SL74HC123 will function at 2.0 V but for optimum pulse width stability, V_{CC} should be above 3.0 V.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V _{CC} V	Guaranteed Limit			Unit
				25 °C to -55°C	≤85 °C	≤125 °C	
V _{IH}	Minimum High-Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V _{IL}	Maximum Low - Level Input Voltage	V _{OUT} =0.1 V or V _{CC} -0.1 V I _{OUT} ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V _{OH}	Minimum High-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	3.98	3.84	3.7	
			6.0	5.48	5.34	5.2	
V _{OL}	Maximum Low-Level Output Voltage	V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
		V _{IN} =V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA I _{OUT} ≤ 5.2 mA	4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I _{IN}	Maximum Input Leakage Current (A, B, CLR)	V _{IN} =V _{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I _{IN}	Maximum Input Leakage Current (R _X , C _X)	V _{IN} =V _{CC} or GND	6.0	±50	±500	±500	nA
I _{CC}	Maximum Quiescent Supply Current (per Package) Standby State	V _{IN} =V _{CC} or GND Q1 and Q2 = Low I _{OUT} =0μA	6.0	130	220	350	μA
I _{CC}	Maximum Supply Current (per Package) Active State	V _{IN} =V _{CC} or GND Q1 and Q2 = High I _{OUT} =0μA Pins 15 and 7 = 0.5 V _{CC}	6.0	25°C	-45°C to 85°C	-55°C to 125°C	μA
				400	600	800	

SL74HC221

AC ELECTRICAL CHARACTERISTICS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input \overline{A} or \overline{B} to Q or Q (Figures 1 and 3)	2.0	255	320	385	ns
		4.5	50	65	75	
		6.0	45	55	65	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, CLR to Q or Q (Figures 2 and 3)	2.0	215	270	325	ns
		4.5	45	55	65	
		6.0	35	45	55	
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 2 and 3)	2.0	75	95	110	ns
		4.5	16	20	22	
		6.0	14	17	20	
C _{IN}	Maximum Input Capacitance \overline{A} , \overline{B} , CLR C_X , R_X	-	10	10	10	pF
			25	25	25	

C _{PD}	Power Dissipation Capacitance (Per Multivibrator)	Typical @25°C, V _{CC} =5.0 V			pF
	Used to determine the no-load dynamic power consumption: $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$	150			

TIMING REQUIREMENTS ($C_L=50\text{pF}$, Input $t_r=t_f=6.0\text{ ns}$)

Symbol	Parameter	V _{CC} V	Guaranteed Limit			Unit
			25 °C to -55°C	≤85°C	≤125°C	
t _{rec}	Minimum Recovery Time, Inactive to A or B (Figure 2)	2.0	0	0	0	ns
		4.5	0	0	0	
		6.0	0	0	0	
t _w	Minimum Pulse Width, Input A or B (Figure 1)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	20	25	
t _w	Minimum Pulse Width, CLR (Figure 2)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	20	25	
t _r , t _f	Maximum Input Rise and Fall Times, CLR (Figure 2)	2.0	1000	1000	1000	ns
		4.5	500	500	500	
		6.0	400	400	400	
	A or B (Figure 2)	2.0	No Limit			
		4.5				
	6.0					

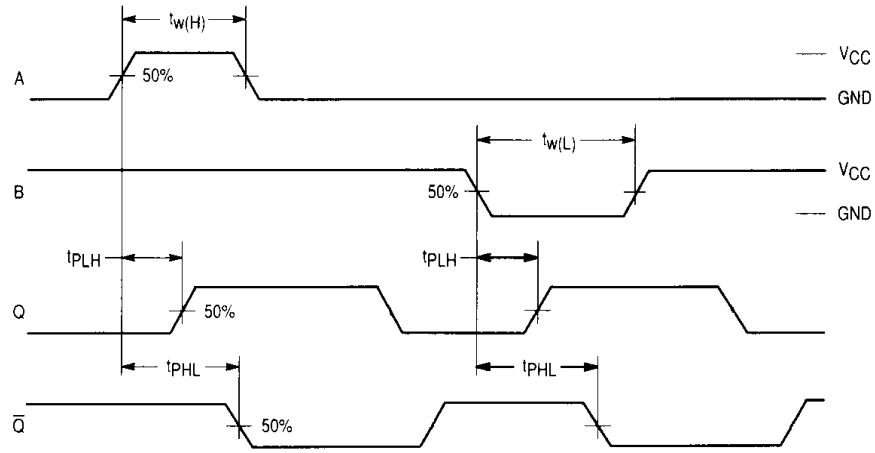


Figure 1. Switching Waveforms

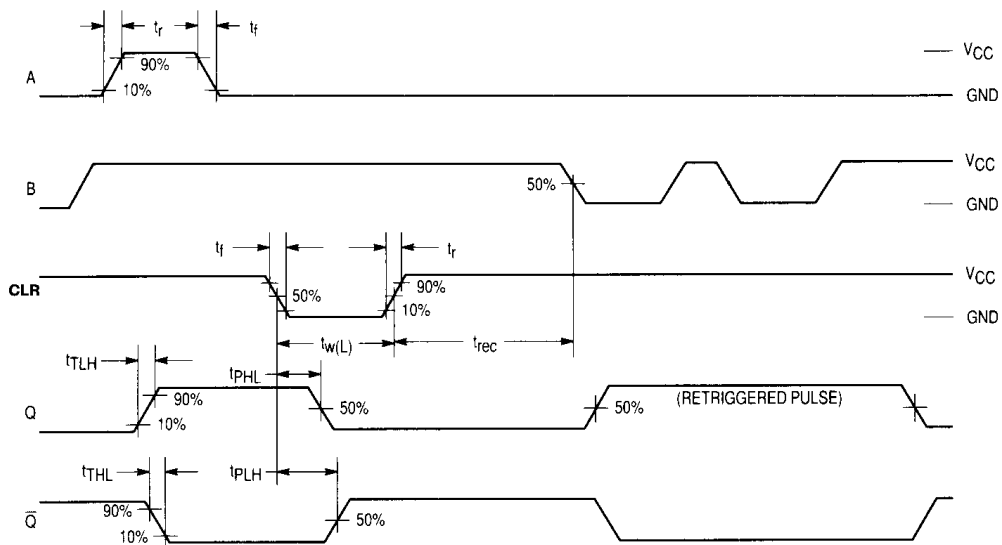
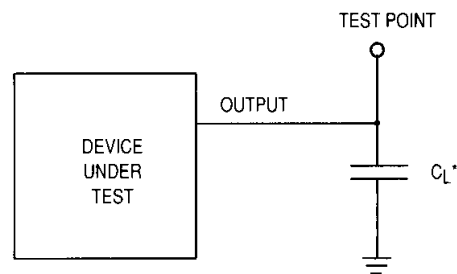


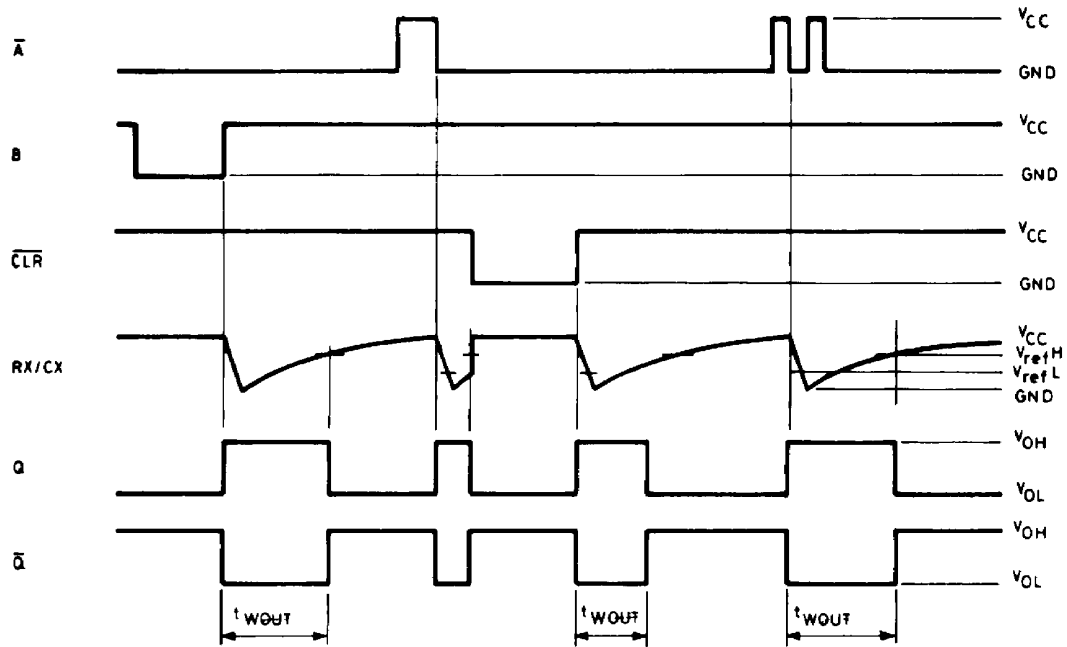
Figure 2. Switching Waveforms



*Includes all probe and jig capacitance

Figure 3. Test Circuit

TIMING DIAGRAM



EXPANDED LOGIC DIAGRAM

